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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/785,373

02/23/2004

Karl M. J. Lofgren

SNDK.015US6

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12/29/2005

PARSONS HSUE & DE RUNTZ LLP
595 MARKET STREET
SUITE 1900
SAN FRANCISCO, CA 94105

EXAMINER

MAI, SON LUU

ART UNIT

PAPER NUMBER

2827

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/785,373	Applicant(s) LOFGREN ET AL.	
	Examiner Son L. Mai	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 September 2005 and 19 December 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 40-54 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 40-54 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>12-19-05</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The papers filed 09-30-05 and 12-19-05 have been received. Claims 40-54 remain pending. The IDS has been considered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 40-54 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As to claims 40, 45 and 51, the specification, as originally filed, lacks support for the following recitations: "enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code" (claim 40), "receiving a portion of an address at the first memory chip and at the second memory chip; comparing the portion of the address to the first selection code and to the second selection code" (claim 45), and "receiving a portion of an address at the first memory chip; enabling the first memory chip if the received address portion matches the first code" (claim 51). Nowhere in the specification mentions about comparing a portion of a received address with a programmable code. The closest explanation about this is found on page 15, paragraph [0069], lines 1-8, "*Device selection by address-matching is*

implemented by a comparator 305 and an address-match latch 307. In order to enable a particular memory device 141, the same address for that device must be obtained from the serial-in lines 237, 239 of the device bus 135. In the present embodiment, a 5-bit array address is shifted into a shift register 311 from the serial-in lines SIO 237, SII 239. The clocking signal is carried in the control line P/D 235 which is gate-enabled by a HIGH signal in the master chip select line CS* 171. The 5-bit array address is then passed from the shift register 311 via the bus 313 to the comparator 305. The comparator 305 compares this address with that obtained from the device-select pinouts 147".* On the contrary, Pruchi et al. (U.S. Patent 6,525,986) discloses in figure 3 and related text at column 6, a portion of a received address is defined as two most significant bits A15 and A16 of bus 72.

Claims 41-44, 46-50, and 52-54 are rejected for depending on the rejected claims 40, 45, and 51, respectively.

Response to Arguments

4. Applicant's arguments filed 09-30-05 have been fully considered but they are not persuasive. On page 5 of the Remarks, the Applicants argued that the specification supports what is claimed, "the description of paragraph (0075) on the address shift register 333 its use for supplying the address on the chip to the 18-bit address bus internal to the chip. Of the entire address, consisting of the array address and the address on the array, it is only this first portion of a received address, the (here) 5-bit array address, that is compared with the first and second codes". On the contrary, as shown in figures 5A and 6A of the instant application, a device select circuit 203 and an internal address bus require two different buses, namely bus 313 (figure 5A) and bus

343 (figure 6A); therefore the bus 313 cannot contain a portion of the received address on the internal address bus 343. They are two different sets of data coming from a same serial lines SI0 and SI1.

Interference

5. Claims 40-54 of this application has been copied by the applicant from U. S. Patent No. 6,525,986. The examiner does not consider this claim to be directed to the same invention as the patent because the claims lack support for the claimed subject matter. Accordingly, interference cannot be initiated based upon this claim.

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on 8am to 6pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



12-23-05

Son L. Mai
Primary Examiner
Art Unit 2827